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	INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	10/086,376
	Date Submitted: June 13, 2002		Filing Date	02/5/2002
			First Named Inventor	Igor KOUZNETSOV et al.
			Group Art Unit	2821
		Examiner Name	Unassigned	
		Attorney Docket Number	035905-0118	

## U.S. PATENT DOCUMENTS

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
LP	B1	4,500,905		Shibata		
	B2	6,185,122		Johnson et al.		
	B3	3,414,892		McCormack et al.	12/13/1968	
	B4	3,432,827		Sarno	3/11/1969	
	B5	4,535,424		Reid		
	B6	4,830,096		Drye		
	B7	4,672,577		Hirose		
	B8	4,710,798		Marcantonio		
	B9	4,811,082		Jacobs		
	B10	5,001,539		Inoue et al.		
	B11	5,089,862		Warner, Jr. et al.		
	B12	5,160,987		Pricer et al.		
	B13	5,191,405		Tomita et al.		
	B14	5,202,754		Bertin et al.		
	B15	5,266,912		Kledzik		
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	B17	5,398,200		Mazure et al.		
	B18	5,422,435		Taklar et al.		
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	B20	5,434,745		Shokrgozar et al.		
	B21	5,453,952		Okudaira		
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	B30	5,552,963		Burns		
	B31	5,561,622		Bertin et al.		
	B32	5,581,498		Ludwig et al.		
	B33	5,585,675		Knopf		
	B34	6,612,570		Eide et al.		
	B35	5,654,220		Leedy		
	B36	5,693,552		Hsu		
	B37	5,696,031		Wark		
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✓	B42	5,915,187		Leedy		

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First Named Inventor	Igor KOUZNETSOV et al.
Group Art Unit	2821
Examiner Name	Unassigned
Attorney Docket Number	035905-0118

## U.S. PATENT DOCUMENTS

		U.S. Patent Document			
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		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
LP	B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982		
	B61	JP	61-222216		Yohehara	10-2-1986		
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		Attorney Docket Number	035905-0118
Sheet	3	of	7

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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	B75	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189	
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	B78	TOSHIO WADA et al.: "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, October 1978, Vol. SC-13, No. 5, pages 635-639	
	B79	CAMPERI-GINESTET C.: "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry", IEEE Photonics Technology Letters, Vol. 4, No. 9, September 1992, pgs. 1003-1006.	
	B80	AKASAKA YOICHI: "Three-dimensional Integrated Circuit: Technology and Application Prospect", Microelectronics Journal, Vol. 20, No.s 1-2, 1989, pgs. 105 - 112.	
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Application Number	10/066,376
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First Named Inventor	Igor KOUZNETSOV et al.
Group Art Unit	2821
Examiner Name	Unassigned
Attorney Docket Number	035905-0118

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	†
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	B84	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	
	B85	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	
	B86	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	
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	B88	WATANABE HIDEHIRO: "Stacked Capacitor Cells for High-density Dynamic RAMs", IEDM, 1988, pgs. 600 - 603.	
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LP ↓ ↓ ↓	B119	Patent Application, AKRAM, US 2002/0030262 A1.	
	B120	Patent Application, AKRAM, US 2002/0030263 A1.	
	B121	Patent Application, LEEDY, US 2001/0033030 A1.	
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: September 20, 2002

(use as many sheets as necessary)

1 of 1

**Complete if Known**

<b>Application Number</b>	10/066,376
<b>Filing Date</b>	02/05/2002
<b>First Named Inventor</b>	Igor G. KOUZNETSOV
<b>Group Art Unit</b>	2823
<b>Examiner Name</b>	Not Assigned
<b>Attorney Docket Number</b>	035805-0118

## U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
LP ↓	C1	6,110,278		Saxena	8/29/2000	
	C2	RE37,259 E		Ovshinsky	7/3/2001	
	C5	0055838A1		Walker et al	12/27/2001	
	C8	0028541A1		Lee et al	03/07/2002	

## FOREIGN PATENT DOCUMENTS

[illegible]

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
LP	C3	"3D Chip-On-Chip Stacking," Semiconductor International, December 1991	
LP	C4	RICHARD W. LAY: "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1994	

Examiner Signature	Long Pham	Date Considered	7/22/04
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	10/068,376
Date Submitted: April 5, 2002		Filing Date	February 5, 2002
(use as many sheets as necessary)		First Named Inventor	Igor KOUZNETSOV et al.
Sheet 1 of 1		Group Art Unit	2823
		Examiner Name	Unassigned
		Attorney Docket Number	035905-0118

## U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code* (if known)			
LP	A127	6,208,645		Leedy	3/27/2001	

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>2</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code* (if known)				

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